IN THE CLAIMS:

Claims 61, 66, and 71 have been amended herein. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1-60. (canceled)

61. (currently amended) A process for fabricating a capacitor on a substrate, said process comprising the steps of:

providing a first insulating layer on said substrate, said first insulating layer having an opening therein forming a container;

forming a generally conformal first conductive layer, having a second etch rate, over said first insulating layer and in said container;

forming a second insulating layer over the entire said first conductive layer; and

removing a portion of said second insulating layer overlying an uppermost portion of portion of said first conductive layer through use of chemical mechanical planarization until said uppermost portion of said first conductive layer is exposed.

62. (original) The process of claim 61, further comprising the step of removing at least a portion of said upper portion of said first conductive layer until said first insulating layer is exposed.

63. (original) The process of claim 61, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

64. (original) The process of claim 61, wherein said first and said second insulating layers are oxides.

65. (original) The method of claim 61, wherein said first insulating layer is subject to a first etch rate and said second insulating layer is subject to a second etch rate, and wherein said first etch rate is a lower etch rate than said second etch rate.

66. (currently amended) A process for fabricating a DRAM containing storage capacitor on a silicon substrate having an existing topography including active areas, word lines and digit lines, said process comprising the steps of:

providing a first insulating layer having a first etch rate, over said existing topography;

forming an opening into said first insulating layer, said opening thereby forming a container;

forming a conformal first conductive layer over said first insulating layer and said container, thereby lining said container;

forming a second insulating layer, having a second etch rate, over the entire said first conductive layer; and

removing said second insulating layer through use of chemical mechanical planarization until an uppermost portion of said first conductive layer is exposed.

67. (original) The process of claim 66, further comprising the step of removing at least a portion of said upper portion of said first conductive layer until said first insulating layer is exposed, thereby forming a conductive container having inner and outer walls.

68. (original) The process of claim 66, wherein said second insulating layer is a sacrificial layer conducive to said chemical mechanical planarization.

69. (original) The process of claim 66, wherein said first and said second insulating layers are oxides.

70. (original) The method of claim 66, wherein said first insulating layer etch rate is a lower etch rate than said second insulating layer etch rate.

71. (currently amended) A process for fabricating a DRAM container storage capacitor on a silicon substrate having an existing topography including active areas, word lines and digit lines, said process comprising the steps of:

providing a first insulating layer, having a first etch rate, over said existing topography;

forming an opening into said first insulating layer, said opening thereby forming a container;

forming a conformal first conductive layer over said first insulating layer and said container, thereby lining said container;

forming a second insulating layer, having a second etch rate, over the entire said first conductive layer; and

removing said second insulating layer through use of chemical mechanical planarization until an uppermost portion of said first conductive layer is exposed;

removing at least a portion of said upper portion of said first conductive layer until said first insulating layer is exposed, thereby forming a conductive container having inner and outer walls.

REMARKS

The Final Office Action mailed March 18, 2004, has been received and reviewed. Claims 61 through 71 are currently pending in the application. Claims 61 through 71 stand rejected. Applicants propose to amend claims 61, 66, and 71, and respectfully request reconsideration of the application as proposed to be amended herein.

Reissue Oath/Declaration

The reissue oath/declaration filed with this application has been objected to as being defective because it fails to contain a statement that all errors which are being corrected in the reissue application up to the time of filing of the oath/declaration arose without any deceptive intention on the part of the Applicants. A Supplemental Reissue Declaration will be filed upon indication of allowable subject matter.

Claim Amendments

The following represents changes to the claims relative to the previously submitted version of the claims in the amendment to the Office Action dated October 21, 2003:

61. (currently amended) A process for fabricating a capacitor on a substrate, said process comprising the steps of:

providing a first insulating layer on said substrate, said first insulating layer having an opening therein forming a container;

forming a generally conformal first conductive layer, having a second etch rate, over said first insulating layer and in said container;

forming a second insulating layer ~~above~~ over the entire said first conductive layer; and

removing ~~at least~~ a portion of said second insulating layer overlying an uppermost portion of portion of said first conductive layer through use of chemical mechanical planarization until ~~an~~ said uppermost portion of said first conductive layer is exposed.

66. (currently amended) A process for fabricating a DRAM containing storage capacitor on a silicon substrate having an existing topography including active areas, word lines and digit lines, said process comprising the steps of:

providing a first insulating layer having a first etch rate, over said existing topography;

forming an opening into said first insulating layer, said opening thereby forming a container;

forming a conformal first conductive layer over said first insulating layer and said container, thereby lining said container;

forming a second insulating layer, having a second etch rate, over the entire said first conductive layer; and

removing said second insulating layer through use of chemical mechanical planarization until an uppermost portion of said first conductive layer is exposed.

71. (currently amended) A process for fabricating a DRAM container storage capacitor on a silicon substrate having an existing topography including active areas, word lines and digit lines, said process comprising the steps of:

providing a first insulating layer, having a first etch rate, over said existing topography;

forming an opening into said first insulating layer, said opening thereby forming a container;

forming a conformal first conductive layer over said first insulating layer and said container, thereby lining said container;

forming a second insulating layer, having a second etch rate, over the entire said first conductive layer; and

removing said second insulating layer through use of chemical mechanical planarization until an uppermost portion of said first conductive layer is exposed;

removing at least a portion of said upper portion of said first conductive layer until said first insulating layer is exposed, thereby forming a conductive container having inner and outer walls.

The above claim changes are supported by Column 2, Lines 50-54; Column 5, Lines 11-13; and Figure 4.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,150,276 to Gonzalez et al.

Claims 61 through 71 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Gonzalez et al. (U.S. Patent No. 5,150,276). Applicants respectfully traverse this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Amended independent Claims 61, 66, and 71 each require "removing at least a portion of said second insulating layer through use of chemical mechanical planarization until an uppermost portion of said first conductive layer is exposed." Thus, chemical mechanical planarization of a second insulating layer ceases once an uppermost layer of the first conductive layer is reached or exposed.

The Examiner relies on Gonzales et al. for disclosure of a method for forming a capacitor including the steps of forming a first insulating layer 40 having an opening 55 on a substrate (Fig. 3 and related text), forming a first conductive layer 60 over the first insulating layer 40 and

within opening 55, and forming a second insulating layer 65 over the first conductive layer 60 (Fig. 4 and related text), all of which are also requirements of Claims 61, 66, and 71. Gonzales et al., however, does not disclose removing a portion of second insulating layer 65 through use of chemical mechanical planarization until an upper portion of the first conductive layer 60 is exposed. The Examiner relies on Fig. 7B of Gonzales et al. (and related text) as supporting the disclosure of this last element of the claims. (Office Action at pages 4 and 6-7). Fig. 7B, however, shows the removal of the entire horizontal layer of first conductive layer 60 so as to totally eliminate the same, as opposed to the removal of second insulating layer 65 (shown in Fig. 4) down to an uppermost layer of first conductive layer 60, as required by the claims of the present application.

Alternatively, Gonzales et al. does disclose selective etching of various layers overlying conductive layer 60 (including second insulating layer 65), as illustrated in Fig. 7A. While this particular method does preserve an upper layer of conductive layer 60, the embodiment of Fig. 7A does not contemplate chemical mechanical planarization (or any other form of planarization) since this particular method of fabrication involves selective etching down to an uppermost layer of conductive layer 60. Significantly, this results in other layers (e.g., second insulating layer 65) remaining in multi-layered or non-planarized forms. Thus, chemical mechanical planarization, as required by the claims of the present application, is not disclosed.

In sum, Gonzales et al. does not disclose a process for fabricating a capacitor on a substrate, which process comprises removing a portion of a second insulating layer through use of chemical mechanical planarization until an uppermost portion of the first conductive layer is exposed. In view of the foregoing, reconsideration and withdrawal of the Section 102(e) rejection of Claims 61, claims 62-65 that depend therefrom, claim 66, claims 67-70 that depend therefrom, and claim 71 under 35 U.S.C. § 102(e) is respectfully requested.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,364,809 to Kwon et al. in View of U.S. Patent No. 5,150,276 to Gonzalez et al.

Claims 61 through 71 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Kwon et al.(U.S. Patent No. 5,364,809) in view of Gonzalez et al. (U.S. Patent No. 5,150,276). Applicants respectfully traverse this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections of claims 61-71 are improper because the combined references do not teach or suggest all of the claim limitations.

In rejecting the claims, the Examiner contends that Kwon et al. discloses the claimed process for forming a capacitor including the step of forming a conformal first conductive layer 48 over the first insulating layer 46 and in the container 54, forming a second insulating layer 50 above the first conductive layer 48, and removing at least a portion of the second insulating layer 50 until an upper portion of the first conductive layer 48 is exposed.

Independent Claims 61, 66, and 71 each require forming a second insulating layer over an entire first conductive layer. This step expressly requires that a second insulating layer be formed over the entire first conductive layer, and not a portion of said layer. Additionally, as previously discussed, independent claims 61, 66 and 71 each require "removing a portion of said second insulating layer through use of chemical mechanical planarization until an uppermost portion of said first conductive layer is exposed." Thus, according to the plain language of the claims, the chemical mechanical planarization of a second insulating layer ceases once an uppermost layer of the first conductive layer is reached or exposed.

The portions of Kwon et al. cited by the Examiner (Figs. 2-4 and related text on cols. 2-3) describe a method of fabricating a capacitor wherein a first polysilicon layer 48 is formed over a substrate 26. Thereafter, a second photoresist 50 is formed over the first polysilicon layer 48 to partially cover the polysilicon layer 48. Thus, portions of polysilicon layer 48 are left uncovered and exposed. Portions of second photoresist 50 are then removed to form openings 56 (Fig. 4D) within electrode regions 54 (shown in Fig. 4B).

Kwon et al. neither teaches nor suggests forming a second insulating layer above an entire first conductive layer, as required by the claims of the present invention. Likewise, the step of removing a portion of said second insulating layer through use of chemical mechanical planarization is not taught or suggested in Kwon et al. In fact, Kwon et al. teaches away from planarization, instead teaching a method of etching back portions of the second photoresist 50 to form openings 56 within a portion of photoresist 50. Notably absent from Kwon et al. is any suggestion to planarize a second insulating layer (i.e., photoresist 50) through use of a chemical mechanical planarization until an uppermost portion of a first conductive layer (i.e., first polysilicon layer 48) is exposed. According to the disclosure in Kwon et al., such a step is, in fact, impossible to carry out since the first conductive layer is never fully covered and, most significantly, since the uppermost portions of first polysilicon layer 48 are removed, as shown in and described with reference to Fig. 4D. Thus, removal of a second insulating layer until an uppermost portion of said first conductive layer is exposed is unnecessary because the upper portion of the first conductive layer is already exposed and, in fact, subsequent use of chemical mechanical planarization are shown to remove the uppermost portions of the first conductive layer.

In view of the foregoing, reconsideration and withdrawal of the Section 103 rejection of Claims 61, claims 62-65 that depend therefrom, claim 66, claims 67-70 that depend therefrom, and claim 71 is respectfully requested.